AMENDMENTS TO THE CLAIMS

1. – 35. (Cancelled).

36. (Original) An integrated circuit device wherein said device is selectively etched by a method, comprising:

placing said device into a reactive chamber;

introducing into said chamber an etching gas;

providing a DC bias voltage to said substrate; and

modulating said DC bias voltage from a first voltage to a second voltage for a predetermined pulsing period to selectively etch said device.

37. (Original) The device according to claim 36, wherein said method includes controlling deposition on a first position of a first material having a first aspect ratio while continuously etching a second position of a second material with a second aspect ratio, wherein said first aspect ratio is less than said second aspect ratio.

38. (Original) The device according to claim 37, wherein said first aspect ratio is less than or equal to 5.

39. (Original) The device according to claim 37, wherein said second aspect ratio is greater than or equal to 3.

40. (Original) The device according to claim 38, wherein said first aspect ratio is from about 0.5 to about 5.0.

41. (Original) The device according to claim 39, wherein said second aspect ratio is from about 3.0 to about 20.0.

42. (Original) The device according to claim 36, wherein said etching gas includes a fluorocarbon gas.

43. (Original) The device according to claim 36, wherein said etching gas includes a hydcrofluorocarbon gas.

44. (Original) The device according to claim 36, wherein said etching gas includes a gas selected from the group consisting of CF4, C2F6, C3F8, C4F8 and CHF3.

45. (Original) The device according to claim 43, wherein said etching gas includes CHF3.

46. (Original) The device according to claim 36, wherein said device includes a self-aligned contact etched thereon.

47. (Original) The device according to claim 36, wherein said bias voltage is modulated on a duty cycle of from about 10 % to about 90%

48. (Original) The device according to claim 36, wherein said modulated DC bias voltage is obtained by modulating a source power.

49. (Original) The device according to claim 36, wherein said modulated DC bias voltage is obtained by modulating a source power, a bias power or combinations thereof.

50. (Original) The device according to claim 36, wherein said predetermined pulsing period is calculated according to a first relative deposition rate and a first relative etch rate of said first material, and to a

second relative deposition rate and a second relative etch rate of said second material.

51. (Original) The device according to claim 36, wherein said bias voltage is modulated between about 0 volts and about 300 volts.

52. (Original) The device according to claim 51, wherein said bias voltage is modulated between about 10 volts and about 80 volts.

53. (Currently Amended) An apparatus for aspect controlled selective etching comprising[[;]]:

a plasma etching chamber including a supported electrode;

a plasma induced bias voltage on said electrode; and

a bias voltage modulator for modulating the DC bias voltage between a first voltage and a second voltage, wherein said first voltage is greater than the voltage at which no etching occurs and said second voltage less that the voltage at which no etching occurs.

54. (Original) The apparatus according to claim 53, wherein said apparatus is a high voltage plasma apparatus.

55. (Original) The apparatus according to claim 53, wherein said high power plasma apparatus has a source power of from about 400 to about 1500 watts.

56. (Original) The apparatus according to claim 54, wherein said apparatus is an inductively coupled plasma apparatus.

57. (Original) The apparatus according to claim 54, wherein said apparatus is an electron cyclotron resonance apparatus.

58. (Original) The apparatus according to claim 53, wherein said apparatus operates at a pressure of from about 2 to about 40 mTorr.

59. (Original) The apparatus according to claim 53, wherein said bias voltage modulator has a duty cycle of from about 10% to about 90%.

60. (Original) The apparatus according to claim 53, wherein said bias voltage is varied from between about 0 volts and about 300 volts.

61. (Original) The apparatus according to claim 53, wherein said plasma is a fluorocarbon gas provided to said reactive plasma chamber by a plasma source.

62. (Original) The apparatus according to claim 53, wherein said bias voltage modulator modulates the source power.

63. (Original) The apparatus according to claim 53, wherein said bias voltage modulator modulates the bias power.

64. (New) A method of forming an integrated circuit device comprising:

forming at least one layer of material to be etched over a substrate;

forming an opening in said at least one layer of material; and

applying a plasma-inducing voltage to said device to deposit a protective layer of material at a first portion of said opening having a first aspect ratio while concurrently etching a second portion of said opening having a second aspect ratio.

65. (New) The method according to claim 64 wherein said first aspect ratio is smaller than said second aspect ratio.

66. (New) The method according to claim 64 wherein said first aspect ratio is from about 0.5 to about 5.0.

67. (New) The method according to claim 64 wherein said protective layer is formed over a gate stack.

68. (New) The method according to claim 64 wherein said second aspect ratio is from about 3.0 to about 20.0.

69. (New) The method according to claim 64 further comprising alternating said voltage between at least a first voltage value and a second voltage value different from said first voltage value.

70. (New) A method of protecting a structure in an integrated circuit during etching comprising:

forming an opening over at least a portion of the structure to be protected; and

applying a plasma-inducing voltage to said integrated circuit whereby a protective layer is deposited onto a first area of said opening which is over said portion of the structure to be protected, while a second area of said opening is continuously etched.

71. (New) The method according to claim 70 wherein said structure to be protected is a gate stack.

72. (New) The method according to claim 70 wherein said first area has a first aspect ration and said second area has a second aspect ratio.

73. (New) The method according to claim 72 wherein said first aspect ratio is smaller than said second aspect ratio.

74. (New) The method according to claim 70 further comprising alternating said voltage between at least a first voltage value and a second voltage value different from said first voltage value.